ABSTRACT

[00112] The present invention provides an architecture code 20 including object circuit information 23 for mapping an object circuit that is at least part of a circuit for executing an application onto part of a logic circuit where circuits can be dynamically reconfigured, interface circuit information 24 for mapping an interface circuit in contact with the object circuit onto the logic circuit, and boundary condition 26 to be realized in the interface circuit. A data processing system in the present invention includes a load unit obtaining an architecture code 20, a mapping unit for mapping the object circuit and the interface circuit in contact with the object circuit onto the logic circuit region according to the object circuit information 23 and the interface circuit information 24 of the architecture code, and a behavior control unit for controlling the interface circuit according to the boundary condition 26 of the architecture code.